WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a plurality of word lines;

a plurality of bit lines;

a memory cell array including memory cells arranged in a matrix shape at the intersections of said plurality of word lines and said plurality of bit lines;

a write circuit arranged per a bit line or a plurality of bit lines in order to perform batch write operation to a page including said plurality of memory cells, said write circuit comprising a plurality of latch circuits for storing data written to a plurality of pages, and bit line connection circuits for connecting said plurality of latch circuits and bit lines;

a voltage generating circuit for generating a voltage necessary for write operation; and

a control circuit for performing write operation to a plurality of pages by repeating continuous program operation which sequentially selects data written to a plurality of pages stored in said plurality of latch circuits while continuously operating said voltage generating circuit to cause the circuit to continuously generate a voltage necessary for program operation thereby continuously performing program operation on a plurality

of pages, and continuous verify operation which sequentially selects data written to a plurality of pages stored in said plurality of latch circuits while continuously operating said voltage generating circuit to cause the circuit to continuously generate a voltage necessary for verify operation thereby continuously performing verify operation on a plurality of pages.

2. A nonvolatile semiconductor memory device according to claim 1, wherein the nonvolatile semiconductor memory device further comprises a control circuit for setting write data to the latch circuits other than that for a selected page during program operation or verify operation of write data stored in the latch circuit for the selected page.

3. A nonvolatile semiconductor memory device according to claim 1, wherein the nonvolatile semiconductor memory device further comprises a level shift circuit for converting the output voltage level of said latch circuit to a high voltage level between said plurality of latch circuits and said bit line connection circuits.

4. A nonvolatile semiconductor memory device according to claim 1, wherein the nonvolatile semiconductor memory device further comprises a detection circuit for

detecting that memory cells are properly programmed during verify operation, a plurality of latch data reset circuits capable of individually resetting latch data in said plurality of latch circuits, and latch data reset selection circuits for selecting a predetermined latch data reset circuit in order to reset latch data in a predetermined latch circuit in case said detection circuit has detected that the memory cells are properly programmed.

5. A nonvolatile semiconductor memory device comprising:

a plurality of word lines;

a plurality of bit lines;

a memory cell array including memory cells arranged in a matrix shape at the intersections of the plurality of word lines and the plurality of bit lines;

a write circuit arranged per a bit line or a plurality of bit lines in order to perform batch write operation to a page including the plurality of memory cells, the write circuit comprising a serial connection latch group where a plurality of latch circuits are connected serially to store data written to a plurality of pages, and a bit line connection circuit for connecting the latch circuit in the final stage of the serial connection latch group and bit lines;

a voltage generating circuit for generating a voltage

necessary for write operation;

a latch data transfer control circuit for transferring latch data in each circuit of the serial connection latch group in a ring shape by transferring latch data in each latch circuit of the serial connection latch group to the latch circuit in the next stage and transferring latch data in the latch circuit in the final stage to the latch circuit in the first stage; and

a control circuit for performing write operation to a plurality of pages by repeating continuous program operation on a plurality of pages which transfers in a ring shape the data written to a plurality of pages stored in the plurality of latch circuits while continuously operating the voltage generating circuit to cause the circuit to continuously generate a voltage necessary for program operation thereby continuously performing program operation on a plurality of pages, and continuous verify operation on a plurality of pages which transfers in a ring shape the data written to a plurality of pages stored in the plurality of latch circuits while continuously operating the voltage generating circuit to cause the circuit to continuously generate a voltage necessary for verify operation thereby continuously performing verify operation on a plurality of pages.

6. A nonvolatile semiconductor memory device according to claim 5, wherein the nonvolatile semiconductor memory device further comprises a control circuit for setting write data to the latch circuits other than that for said selected page during program operation or verify operation of write data stored in the latch circuit for the selected page.

7. A nonvolatile semiconductor memory device according to claim 5, wherein the nonvolatile semiconductor memory device further comprises a level shift circuit for converting the output voltage level of said latch circuit in the final stage to a high voltage level between the latch circuit in the final stage of said serial connection latch group and said bit line connection circuit.

8. A nonvolatile semiconductor memory device according to claim 5, wherein the nonvolatile semiconductor memory device further comprises a detection circuit for detecting that memory cells are properly programmed during verify operation and a latch data reset circuit for resetting the latch data in the latch circuit in the final stage of said serial connection latch group in case said detection circuit has detected that the memory cells are properly programmed.

9. A nonvolatile semiconductor memory device according to claim 1, wherein said plurality of latch circuits comprise flip-flop circuits.

10. A nonvolatile semiconductor memory device according to claim 1, wherein the nonvolatile semiconductor memory device further comprises a control circuit for performing continuous program operation and continuous verify operation on the pages where write data setting is complete, said page being other than said selected page, until setting of write data to the latch circuit for said selected page is complete, while setting write data to the latch circuit for the selected page.

11. A nonvolatile semiconductor memory device according to claim 1, wherein the nonvolatile semiconductor memory device further comprises a control circuit for skipping program operation and verify operation on said selected page and performing program operation and verify operation on the next page in case the write data stored in the latch circuit for the selected page contains no program data.

12. A nonvolatile semiconductor memory device

according to claim 1, wherein the nonvolatile semiconductor memory device further comprises a control circuit for setting data written to a new page to the latch circuit for a page where said write operation is complete during the subsequent program operation or verify operation on the next page in case it has been detected that the memory cells for said selected page are properly programmed in the verify operation on the selected page.

13. A nonvolatile semiconductor memory device according to claim 1, said memory cell array comprising memory cells for a plurality of pages connected to a single word line, wherein the nonvolatile semiconductor memory device further comprises a control circuit for performing said continuous program operation with a voltage necessary for program operation continuously applied to said word line.

14. A nonvolatile semiconductor memory device according to claim 1, said memory cell array comprising memory cells for a plurality of pages connected to a single word line, wherein the nonvolatile semiconductor memory device further comprises a control circuit for performing said continuous verify operation with a voltage necessary for verify operation continuously applied to said word line.

15. A nonvolatile semiconductor memory device according to claim 1, said memory cell array comprising memory cells for a plurality of pages connected to a single word line, wherein the nonvolatile semiconductor memory device further comprises a bit line reset circuit for setting non-selected bit lines to a ground potential during said continuous program operation or said continuous verify operation.

16. A method of writing to a nonvolatile semiconductor memory device comprising: a plurality of word lines; a plurality of bit lines; a memory cell array including memory cells arranged in a matrix shape at the intersections of said plurality of word lines and said plurality of bit lines; a write circuit arranged per a bit line or a plurality of bit lines, said write circuit comprising a plurality of latch circuits for storing data written to a plurality of pages, and a bit line connection circuit for connecting said plurality of latch circuits and bit lines in order to perform batch write operation to a page including said plurality of memory cells; and a voltage generating circuit for generating a voltage necessary for write operation;

wherein said method performs the following operations:

a continuous program operation on a plurality of pages

which sequentially selects data written to a plurality of pages stored in said plurality of latch circuits while continuously operating said voltage generating circuit to cause the circuit to continuously generate a voltage necessary for program operation thereby continuously performing program operation on a plurality of pages;

a continuous verify operation on a plurality of pages which sequentially selects data written to a plurality of pages stored in said plurality of latch circuits while continuously operating said voltage generating circuit to cause the circuit to continuously generate a voltage necessary for verify operation thereby continuously performing verify operation on a plurality of pages; and

repeating the continuous program operation and the continuous verify operation to thereby perform a write operation to a plurality of pages.

17. A method of writing to a nonvolatile semiconductor memory device according to claim 16, wherein the method sets write data to the latch circuits other than that for said selected page during program operation or verify operation of write data stored in the latch circuit for the selected page.

18. A method of writing to a nonvolatile

semiconductor memory device comprising: a plurality of word lines; a plurality of bit lines; a memory cell array including memory cells arranged in a matrix shape at the intersections of said plurality of word lines and said plurality of bit lines; a write circuit arranged per a bit line or a plurality of bit lines in order to perform batch write operation to a page including said plurality of memory cells, said write circuit comprising a serial connection latch group where a plurality of latch circuits are connected serially to store data written to a plurality of pages, and a bit line connection circuit for connecting the latch circuit in the final stage of said serial connection latch group and bit lines; a latch data transfer control circuit for transferring latch data in each circuit of said serial connection latch group in a ring shape by transferring latch data in each latch circuit of said serial connection latch group to the latch circuit in the next stage and transferring latch data in the latch circuit in the final stage to the latch circuit in the first stage; and a voltage generating circuit for generating a voltage necessary for write operation;

wherein said method performs the following operations:

a continuous program operation on a plurality of pages which transfers in a ring shape the data written to a plurality of pages stored in said plurality of latch circuits while

continuously operating said voltage generating circuit to cause the circuit to continuously generate a voltage necessary for program operation thereby continuously performing program operation on a plurality of pages;

a continuous verify operation on a plurality of pages which transfers in a ring shape the data written to a plurality of pages stored in said plurality of latch circuits while continuously operating said voltage generating circuit to cause the circuit to continuously generate a voltage necessary for verify operation thereby continuously performing verify operation on a plurality of pages; and

repeating the continuous program operation and the continuous verify operation to thereby perform a write operation to a plurality of pages.

19. A method of writing to a nonvolatile semiconductor memory device according to claim 18, wherein write data setting is made to the latch circuits other than that for said selected page during program operation or verify operation of write data stored in the latch circuit for the selected page.

20. A method of writing to a nonvolatile semiconductor memory device according to claim 16, wherein the method performs continuous program operation and

continuous verify operation on the pages where write data setting is complete, said page being other than said selected page, until setting of write data to the latch circuit for said selected page is complete, while setting write data to the latch circuit for the selected page.

21. A method of writing to a nonvolatile semiconductor memory device according to claim 16, wherein the method skips program operation and verify operation on said selected page and performs program operation and verify operation on the next page in case the write data stored in the latch circuit for the selected page contains no program data.

22. A method of writing to a nonvolatile semiconductor memory device according to claim 16, wherein the method sets data written to a new page to the latch circuit for a page where said write operation is complete during the subsequent program operation or verify operation on the next page in case it has been detected that the memory cells for said selected page are properly programmed in the verify operation on the selected page.

23. A method of writing to a nonvolatile semiconductor memory device according to claim 16, said

memory cell array comprising memory cells for a plurality of pages connected to a single word line, wherein the method performs said continuous program operation with a voltage necessary for program operation continuously applied to said word line.

24. A method of writing to a nonvolatile semiconductor memory device according to claim 16, said memory cell array comprising memory cells for a plurality of pages connected to a single word line, wherein the method performs said continuous verify operation with a voltage necessary for verify operation continuously applied to said word line.

25. A nonvolatile semiconductor memory device according to claim 5, wherein said plurality of latch circuits comprise flip-flop circuits.

26. A nonvolatile semiconductor memory device according to claim 5, wherein the nonvolatile semiconductor memory device further comprises a control circuit for performing continuous program operation and continuous verify operation on the pages where write data setting is complete, said page being other than said selected page, until setting of write data to the latch circuit for said

selected page is complete, while setting write data to the latch circuit for the selected page.

27. A nonvolatile semiconductor memory device according to claim 5, wherein the nonvolatile semiconductor memory device further comprises a control circuit for skipping program operation and verify operation on said selected page and performing program operation and verify operation on the next page in case the write data stored in the latch circuit for the selected page contains no program data.

28. A nonvolatile semiconductor memory device according to claim 5, wherein the nonvolatile semiconductor memory device further comprises a control circuit for setting data written to a new page to the latch circuit for a page where said write operation is complete during the subsequent program operation or verify operation on the next page in case it has been detected that the memory cells for said selected page are properly programmed in the verify operation on the selected page.

29. A nonvolatile semiconductor memory device according to claim 5, said memory cell array comprising memory cells for a plurality of pages connected to a single

word line, wherein the nonvolatile semiconductor memory device further comprises a control circuit for performing said continuous program operation with a voltage necessary for program operation continuously applied to said word line.

30. A nonvolatile semiconductor memory device according to claim 5, said memory cell array comprising memory cells for a plurality of pages connected to a single word line, wherein the nonvolatile semiconductor memory device further comprises a control circuit for performing said continuous verify operation with a voltage necessary for verify operation continuously applied to said word line.

31. A nonvolatile semiconductor memory device according to claim 5, said memory cell array comprising memory cells for a plurality of pages connected to a single word line, wherein the nonvolatile semiconductor memory device further comprises a bit line reset circuit for setting non-selected bit lines to a ground potential during said continuous program operation or said continuous verify operation.

32. A method of writing to a nonvolatile semiconductor memory device according to claim 18, wherein the method performs continuous program operation and

continuous verify operation on the pages where write data setting is complete, said page being other than said selected page, until setting of write data to the latch circuit for said selected page is complete, while setting write data to the latch circuit for the selected page.

33. A method of writing to a nonvolatile semiconductor memory device according to claim 18, wherein the method skips program operation and verify operation on said selected page and performs program operation and verify operation on the next page in case the write data stored in the latch circuit for the selected page contains no program data.

34. A method of writing to a nonvolatile semiconductor memory device according to claim 18, wherein the method sets data written to a new page to the latch circuit for a page where said write operation is complete during the subsequent program operation or verify operation on the next page in case it has been detected that the memory cells for said selected page are properly programmed in the verify operation on the selected page.

35. A method of writing to a nonvolatile semiconductor memory device according to claim 18, said

memory cell array comprising memory cells for a plurality of pages connected to a single word line, wherein the method performs said continuous program operation with a voltage necessary for program operation continuously applied to said word line.

36. A method of writing to a nonvolatile semiconductor memory device according to claim 18, said memory cell array comprising memory cells for a plurality of pages connected to a single word line, wherein the method performs said continuous verify operation with a voltage necessary for verify operation continuously applied to said word line.